Amendments to the Claims:

Claims 1-27 (Cancelled)

28. (Currently amended) A circuit, comprising

an encoder circuit coupled to receive a plurality of symbols, the encoder circuit producing the plurality of symbols at a first output terminal and a transform of the plurality of symbols at a second output terminal within a time slot, the encoder circuit producing a sequence of predetermined signals interposed with the plurality of symbols, the encoder circuit coupled to receive a control signal, the encoder circuit producing the plurality of symbols at the first output terminal and the transform of the plurality of symbols at the second output terminal in response to a first value of the control signal, the encoder circuit producing the plurality of symbols at the first output terminal and not producing the transform of the plurality of symbols at the second output terminal in response to a second value of the control signal.

29. (Cancelled)

30. (Currently amended) A circuit as in claim ~~29~~ 28, further comprising a diversity control circuit coupled to receive a first input signal, the diversity control circuit producing the control signal corresponding to the first input signal.

31. (Previously amended) A circuit as in claim 30, wherein the first input signal corresponds to a Doppler frequency.

32. (Previously amended) A circuit as in claim 31, wherein the diversity control circuit is further coupled to receive a second input signal corresponding to a handoff signal.

33. (Previously amended) A circuit as in claim 30, wherein the first input signal corresponds to a handoff signal.

34. (Previously amended) A circuit as in claim 28, wherein the encoder circuit produces a midamble of the predetermined signals interposed with the plurality of symbols.

35. (Original) A circuit as in claim 28, wherein the sequence of predetermined signals comprises a code sequence, and wherein a first shift of the code sequence corresponds to the first output terminal and a second shift of the code sequence corresponds to the second output terminal.

Claims 36-38 (Cancelled)

39. (Original) A circuit, comprising an encoder circuit coupled to receive a plurality of symbols, the encoder circuit producing the plurality of symbols and a sequence of predetermined signals at a first and a second output terminal, wherein the sequence of predetermined signals comprises a code sequence, and wherein a first shift of the code sequence corresponds to the first output terminal and a second shift of the code sequence corresponds to the second output terminal.

40. (Currently amended) A circuit, comprising:

an encoder circuit coupled to receive a plurality of first symbols corresponding to a first user, the encoder circuit producing the plurality of first symbols at a first output terminal and a transform of the plurality of first symbols at a second output terminal within a time slot, the encoder circuit coupled to receive a control signal, the encoder circuit producing the plurality of first symbols at the first output terminal and the transform of the plurality of first symbols at the second output terminal in response to a first value of the control signal, the encoder circuit producing the plurality of first symbols at the first output terminal and not producing the transform of the plurality of first symbols at the second output terminal in response to a second value of the control signal;

a first multiplier circuit coupled to receive the plurality of first symbols and arranged to multiply the plurality of first symbols by a code corresponding to the first user to produce a first coded signal, wherein the first coded signal is applied to a first antenna; and

a second multiplier circuit coupled to receive the transform of the plurality of first symbols and arranged to multiply the transform of the plurality of first symbols by the code corresponding to the first user to produce a second coded signal, wherein the second coded signal is applied to a second antenna.

41. (Previously added) A circuit as in claim 40, comprising a third multiplier circuit coupled to receive a plurality of second symbols and arranged to multiply the plurality of second symbols by a code corresponding to a second user to produce a third coded signal.

42. (Previously added) A circuit as in claim 41, wherein the third coded signal is applied to the first antenna and not the second antenna.

43. (Cancelled)

44. (Currently amended) A circuit as in claim ~~43~~ 40, comprising a diversity control circuit coupled to receive a first input signal, the diversity control circuit producing the control signal corresponding to the first input signal.

45. (Previously added) A circuit as in claim 44, wherein the first input signal corresponds to a Doppler frequency.

46. (Previously added) A circuit as in claim 45, wherein the diversity control circuit is further coupled to receive a second input signal corresponding to a handoff signal.

47. (Previously added) A circuit as in claim 44, wherein the first input signal corresponds to a handoff signal.

48. (Previously added) A circuit as in claim 40, wherein the encoder circuit produces a midamble of predetermined signals interposed with the plurality of first symbols.

49. (Previously added) A circuit as in claim 48, wherein the predetermined signals comprise a code sequence, and wherein a first shift of the code sequence corresponds to the first output terminal and a second shift of the code sequence corresponds to the second output terminal.